FAIRCHILD

SEMICONDUCTOR

DM74LS75 Quad Latch

General Description

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable is HIGH, and the Q output will follow the data input as long as the enable remains HIGH. When the enable goes LOW, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go HIGH.

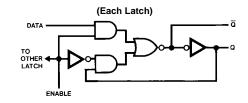
These latches feature complementary Q and \overline{Q} outputs from a 4-bit latch, and are available in 16-pin packages.

Ordering Code:

Order Number	Package Number	Package Description
DM74LS75M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS75N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Diagram



Function Table (Each Latch)

Γ	Inputs		Outputs		
Γ	D	Enable	Q	Q	
	L	Н	L	Н	
	н	н	н	L	
	Х	L	Q ₀	\overline{Q}_0	

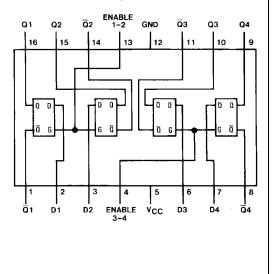
H = HIGH Level

L = LOW Level X = Don't Care

 $Q_0 =$ The Level of Q Before the HIGH-to-LOW Transition of ENABLE

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Connection Diagram



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Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	$0^{\circ}C$ to $+70^{\circ}C$
Storage Temperature Range	-65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V _{CC}	Supply Voltage	4.75	5	5.25	V
VIH	HIGH Level Input Voltage	2			V
V _{IL}	LOW Level Input Voltage			0.8	V
I _{OH}	HIGH Level Output Current			-0.4	mA
OL	LOW Level Output Current			8	mA
^t w	Enable Pulse Width (Note 5)	20			ns
^t su	Setup Time (Note 5)	20			ns
ŀн	Hold Time (Note 5)	0			ns
T _A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
VI	Input Clamp Voltage	$V_{CC} = Min, I_I = -18 \text{ mA}$				-1.5	V
V _{OH}	HIGH Level Output Voltage	$V_{CC} = Min, I_{OH} = Max$ $V_{IL} = Max, V_{IH} = Min$		2.7	3.5		V
V _{OL}	LOW Level Output Voltage	$V_{CC} = Min, I_{OL} = Max$ $V_{IL} = Max, V_{IH} = Min$			0.35	0.5	V
		$I_{OL} = 4 \text{ mA}, V_{CC} = \text{Min}$			0.25	0.4	
l _l	Input Current @ Max	$V_{CC} = Max, V_I = 7V$	D			0.1	mA
	Input Voltage		Enable			0.4	- IIIA
IIH	HIGH Level Input	$V_{CC} = Max, V_I = 2.7V$	D			20	μA
	Current		Enable			80	μΑ
IIL	LOW Level Input	$V_{CC} = Max, V_I = 0.4V$	D			-0.4	mA
	Current		Enable			-1.6	- IIIA
los	Short Circuit Output Current	V _{CC} = Max (Note 2)		-20		-100	mA
I _{CC}	Supply Current	V _{CC} = Max (Note 3)			6.3	12	mA

Note 2: All typicals are at $V_{CC} = 5V$, $T_A = 25^{\circ}C$.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 4: I_{CC} is measured with all outputs open and all inputs grounded.

Note 5: T_A = 25°C and V_{CC} = 5V.

Switc	hing Characteristi	cs					
at $V_{CC} = 5$	V and T _A = 25°C		$R_L = 2 k\Omega$				
Symbol	Parameter	To (Output)	C _L = 15 pF		C _L = 50 pF		
			Min	Max	Min	Ma	
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	D to Q		27		30	
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	D to Q		17		25	
t _{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	D to \overline{Q}		20		25	
t _{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	D to Q		15		20	
t _{PLH}	Propagation Delay Time	Enable to Q		27		30	

Enable to Q

Enable to \overline{Q}

Enable to \overline{Q}

LOW-to-HIGH Level Output Propagation Delay Time

HIGH-to-LOW Level Output Propagation Delay Time

LOW-to-HIGH Level Output

HIGH-to-LOW Level Output

Propagation Delay Time

Г

t_{PHL}

t_{PLH}

t_{PHL}

DM74LS75

Units

ns

ns

ns

ns

ns

ns

ns

ns

Max 30

25

25

20

30

30

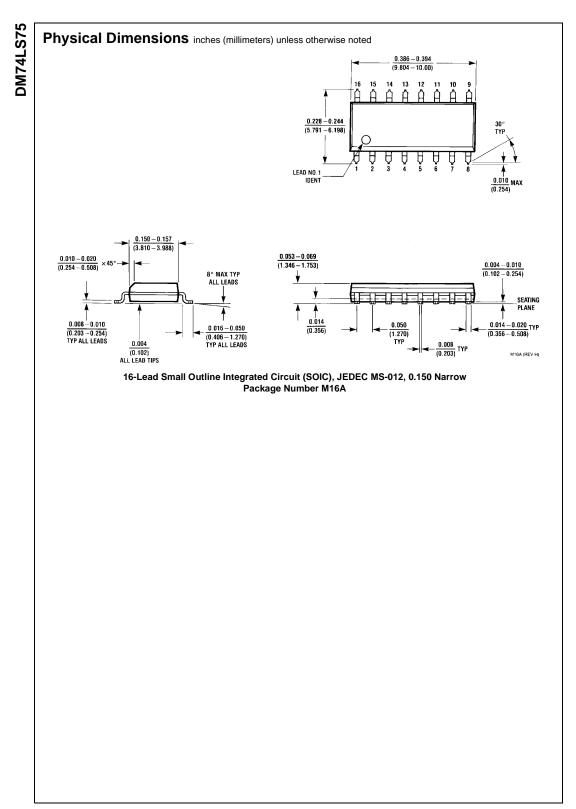
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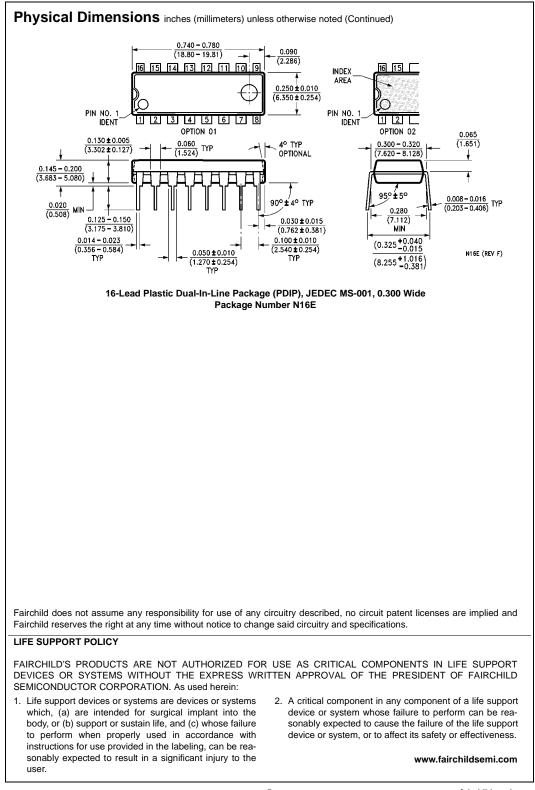
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