

256-bit TTL bipolar PROM (32 x 8)

82S23/S23A/S23B
82S123/123A/123B

APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Format conversion
- Hardwired algorithms
- Random logic
- Code conversion

FEATURES

- Address access time: 50ns max
- Input loading: -150µA max
- On-chip address decoding
- One chip enable input
- Output options:
- 82S23: Open collector
- 82S123: 3-State
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible

DESCRIPTION

The 82S23 and 82S123 are field-programmable, which means that custom patterns are immediately available by following the Philips Generic I fusing procedure. The 82S23 and 82S123 devices are supplied with all outputs at a logical Low. Outputs are programmed to a logic High level at any specified address by fusing a Ni-Cr link matrix.

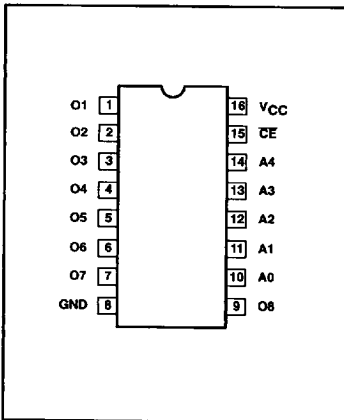
These devices include on-chip decoding and 1 chip enable input for memory expansion. They feature either Open collector or 3-State outputs for optimization of word expansion in bused organizations

ORDERING INFORMATION

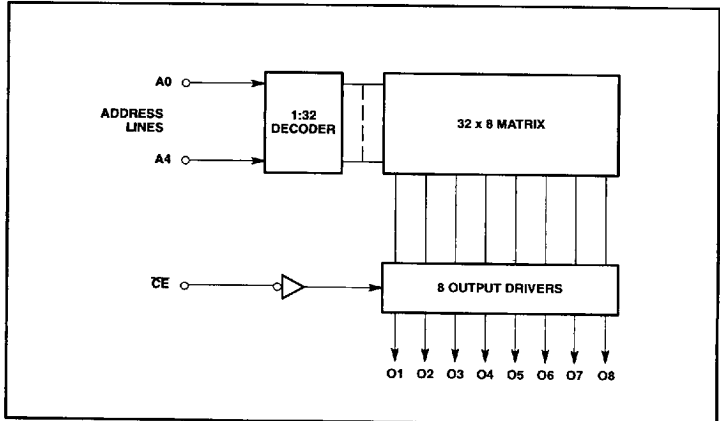
DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
16-Pin Ceramic DIP (300mil-wide)	82S23/BEA	GDIP1-T16
	82S123/BEA	GDIP1-T16
	82S23A/BEA	GDIP1-T16
	82S123A/BEA	GDIP1-T16
	82S23B/BEA	GDIP1-T16
16-Pin Ceramic Flat Pack	82S23/BFA	GDFF2-F16
	82S123/BFA	GDFF2-F16
	82S23A/BFA	GDFF2-F16
	82S123A/BFA	GDFF2-F16
	82S23B/BFA	GDFF2-F16

* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

PIN CONFIGURATION



BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	Supply voltage	+7	V _{DC}
V _I	Input voltage	+5.5	V _{DC}
V _O	Output voltage High (82S23)	+5.5	V _{DC}
V _O	Output voltage Off-State (82S123)	+5.5	V _{DC}
T _A	Operating temperature range	-55 to +125	°C
T _{STG}	Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS

-55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

SYMBOL	PARAMETER	TEST CONDITIONS ^{1, 2}	LIMITS			UNIT
			MIN	TYP ⁵	MAX	
Input voltage						
V _{IL}	Low	V _{CC} = 4.5V, I _I = -18mA	2.0		0.8	V
V _{IH}	High				V	
V _{IK}	Clamp				-1.2	V
Output voltage						
V _{OL}	Low	CE = Low I _O = 16mA I _O = -2mA, V _{CC} = 4.5V	2.4		0.5	V
V _{OH}	High				V	
Input current						
I _{IL}	Low	V _{CC} = 5.5V V _I = 0.45V V _I = 2.7V V _I = 5.5V			-150	μA
I _{IH1}	High				25	μA
I _{IH2}	High				40	μA
Output current¹						
I _{OLK}	Leakage (82S23)	V _{CC} = 5.5V CE = High, V _O = 5.5V CE = High, V _O = 5.5V CE = High, V _O = 0.4V V _{CC} = 5.5V, CE = Low, V _O = 0V, High stored			40	μA
I _{OZ}	Hi-Z state (82S123)				40	μA
I _{OS}	Short circuit (82S123) ³				-40	μA
					-100	mA
Supply current						
I _{CC}		V _{CC} = 5.5V, CE = High			110	mA
Capacitance⁶						
C _{IN}	Input	CE = High, V _{CC} = 5.0V V _I = 2.0V V _O = 2.0V			5	pF
C _{OUT}	Output				8	13

AC ELECTRICAL CHARACTERISTICS

-55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

SYMBOL	PARAMETER	TO	FROM	LIMITS - 82S23/123			UNIT
				MIN	TYP ⁵	MAX	
t _{AA}	Access time ⁴	Output	Address		20	50	ns
t _{CE}	Access time ⁴	Output	Chip Enable			30	ns
t _{CD}	Disable time	Output	Chip Disable			30	ns

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AC ELECTRICAL CHARACTERISTICS

-55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

SYMBOL	PARAMETER	TO	FROM	LIMITS - 82S23A/123A			UNIT
				MIN	TYP ⁵	MAX	
t _{AA}	Access time ⁴	Output	Address		20	35	ns
t _{CE}	Access time ⁴	Output	Chip Enable			22	ns
t _{CD}	Disable time	Output	Chip Disable			22	ns

AC ELECTRICAL CHARACTERISTICS

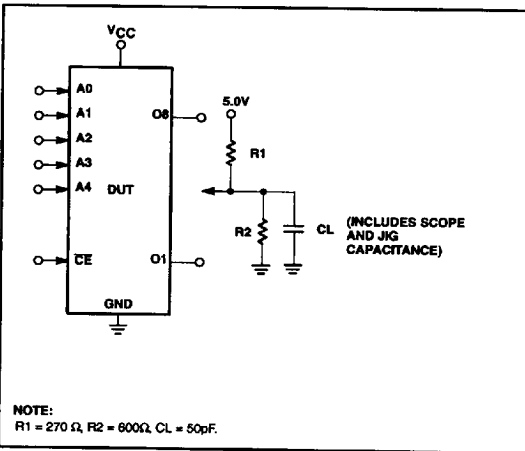
-55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

SYMBOL	PARAMETER	TO	FROM	LIMITS - 82S23B/123B			UNIT
				MIN	TYP ⁵	MAX	
t _{AA}	Access time ⁴	Output	Address		20	30	ns
t _{CE}	Access time ⁴	Output	Chip Enable			18	ns
t _{CD}	Disable time	Output	Chip Disable			18	ns

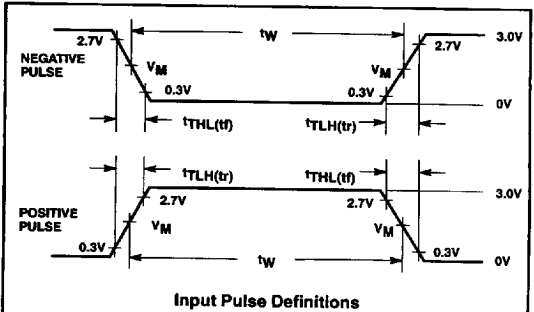
NOTES:

1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at V_{CC} = 5V, T_A = +25°C.
6. Guaranteed, but not tested.

TEST LOAD CIRCUITS



VOLTAGE WAVEFORMS

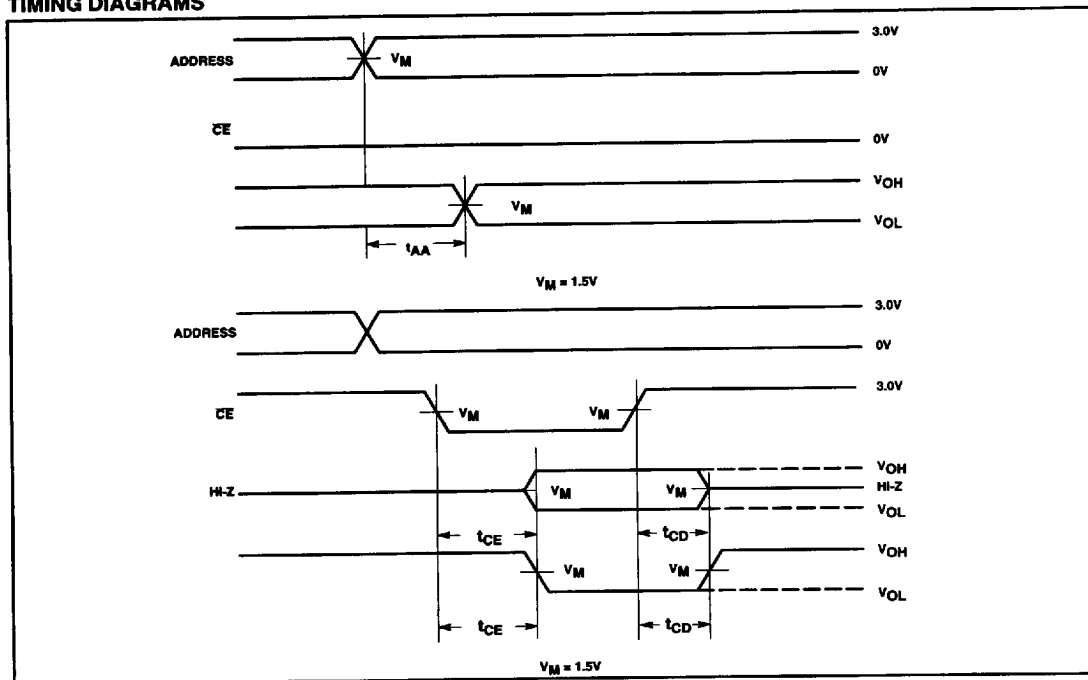


INPUT PULSE CHARACTERISTICS				
V _M	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

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TIMING DIAGRAMS



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