T P G

Test Pattern Generator

Updated 7/12/2017 - Firmware 03
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Usage

The Test Pattern Generator produces display patterns for use with Standard Resolution (15.7khz) and Medium Resolution (24khz) RGB monitors. These patterns may be used to calibrate a display, or diagnose display issues.

FEATURES

- Selectable resolution (Standard/Medium)
- +/- H,V Sync, +/- Composite Sync
- R,G,B Cut-off
- Inverted video support for Sanyo/Sharp monitors
- On Screen Menu for easy pattern/option configuration
- Optional Sleep/Resume function
- On-board firmware programming interface (ISP)
- Powered by 9V battery (not included)
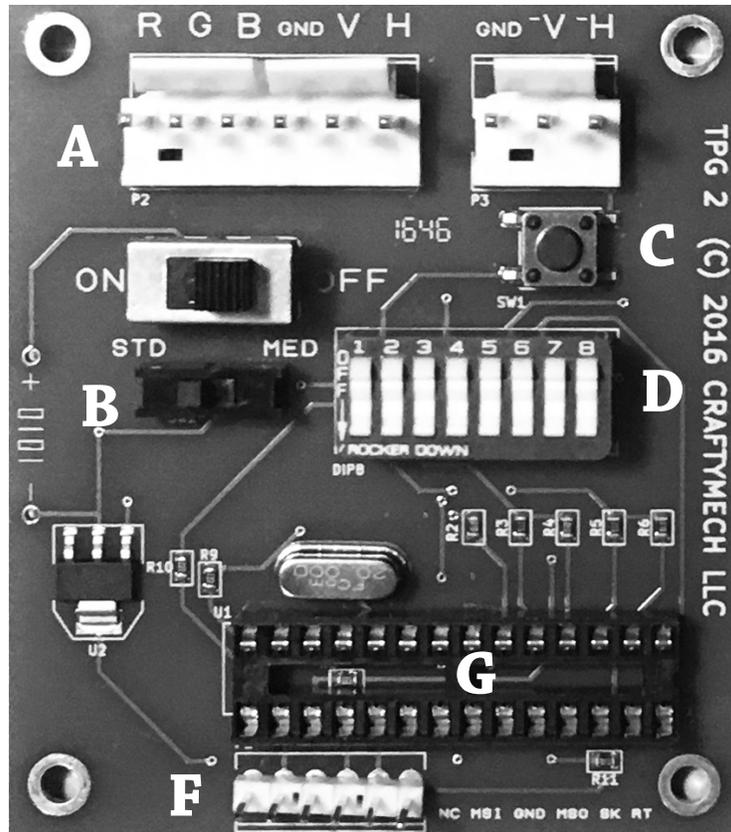
CONTENTS

1: Output Header

The output header is a 10 pin interface for connecting the TPG to a monitor chassis.

The layout from left to right is: R,G,B,GND,V,H,N/C,GND,-V,-H

It is recommended to use a test cable with a 4 position connector for R,G,B,GND and a 2 position connector for the desired sync polarity.

The H output pins may be used for composite sync. In some cases it may be necessary to disable the V output if using H for composite sync (see Section 4, Dip 6). If composite sync output in the H pins is not desired, this option can be disabled from the On Screen Menu (Dip 5=ON).

The connector pins on the output header are .156 pitch. Although separated into two blocks of 6 and 3 pins, the output header will accept a 10 pin connector. However, it will be easier to remove connectors from the output header if they are split into smaller blocks (4 and 2 pins as recommended above).

2: Resolution

The TPG supports Standard Resolution (15.7khz) and Medium Resolution (24khz) modes.

The resolution is selected with slide switch (B), while the unit is powered off. If the resolution is changed while the power is on, the setting will take effect on the next power cycle.

Always double check the resolution switch setting before connecting the TPG to a monitor chassis. Mismatching the resolution & chassis type may result in damage to the chassis when the TPG is powered on.

3: Pattern Selection

Push button (C) is used to select the test pattern to display. Pressing (C) will cycle through the available patterns for the chosen resolution. Holding down (C) will rapidly cycle the available test patterns.

The On Screen Menu (Dip 5=ON) allows individual patterns to be toggled on/off. When cycling through patterns using (C), only enabled patterns will be displayed.

PATTERN LIST

Checkerboard
8 Color Bars + Gray
8 Color Gradient
RGB Color Gradient
RGB Color Bars
Black & White Gradient
Solid Red
Solid Green
Solid Blue
Solid White
Solid Yellow
Solid Gray
Crosshatch w/ center dots
"Falling Blocks" Animation

4: Dip Switches

The TPG's advanced functions are configured via the dip switch bank (D). Dip switches are always in one of two states: ON or OFF. The switch numbers run from left (1) to right (8). A switch is ON, when the top of the rocker switch is depressed. A switch is OFF when the bottom of the rocker switch is depressed.

Dip 1: Red Channel

      OFF: Cut Off (no signal)   ON: Red signal active

Dip 2: Green Channel

      OFF: Cut Off (no signal)   ON: Green signal active

Dip 3: Blue Channel

      OFF: Cut Off (no signal)   ON: Blue signal active

Dip 4: Invert RGB Signal

      OFF: Normal   ON: Inverted

Inverting the RGB will output a signal compatible with Sanyo and Sharp monitors used with Nintendo arcade boards. The overscan area of the video signal is not inverted, so white borders will appear around the test patterns (outside the display area). The title & menu screens are also not inverted.

Dip 5: On Screen Menu *(STD RES ONLY)*

     OFF: Disabled   ON: Enabled

Activating the On Screen Menu will display a configuration screen where individual patterns can be toggled on/off. Advanced functions may also be toggled on/off, such as Sleep/Resume and CSYNC.

See Section 5 for a detailed explanation of the On Screen Menu usage.

Dip 6: VSYNC Off

     OFF: Normal V   ON: V disabled

The setting may be used to disable V output for cases where only H is needed, but the available cable has both H,V pinned. While usually harmless, sync problems may result for some chassis if V is present when using H for composite sync.

Refer to table D.1 for valid combinations of Dips 6,7,8

Dip 7: +H2 *(USE WITH DIP 6=ON)*

     OFF: Normal H   ON: Dual H output

This setting may be used to duplicate +H on the +V output pin. This is useful for cases where +H is needed on both H/V pins for proper sync.

This dip setting should only be used with Dip 6=ON. If VSYNC output is active (Dip 6=OFF), while also duplicating H (Dip 7=ON), the result will be an unusable signal. Refer to table D.1 for valid combinations of Dips 6,7,8

Dip 8: -H2 *(USE WITH DIP 6=ON)*
OFF: Normal -H   ON: Dual -H output

This setting may be used to duplicate -H on the -V output pin. This is useful for cases where -H is needed on both H/V pins for proper sync.

This dip setting should only be used with Dip 6=ON. If VSYNC output is active (Dip 6=OFF), while also duplicating H (Dip 7=ON), the result will be an unusable signal. Refer to table D.1 for valid combinations of Dips 6,7,8

Table D.1 - Valid Combinations of Dip Switches 6,7,8

DIP 6	DIP 7	DIP 8	V,-V Outputs
OFF	OFF	OFF	V= VSYNC, -V= -VSYNC
ON	OFF	OFF	V,-V= No Signal
ON	ON	OFF	V= H pin, -V= No Signal
ON	OFF	ON	V= No Signal, -V= -H

5: On Screen Menu

The On Screen Menu (OSM) is activated by setting Dip 5=ON. The OSM is only supported in STD Resolution, although the settings will carry over to MED Resolution.

The Pattern select button (C) is used to navigate the OSM options. A short press of (C) will move the cursor to the next option, while a longer press of (C) will toggle the option between Y/N.

All patterns except the crosshatch may be disabled from the OSM.

Sleep

The sleep/resume function of the TPG is designed as a battery saving feature if the unit is accidently left on. When enabled, the TPG will enter a low-power state after approximately 30 minutes. Pressing the Pattern Select button (C) will resume operation by displaying the last selected pattern.

The Blocks animation will run indefinitely, and will not respond to the Sleep/Resume function. This mode may be used for "burn" testing of a chassis after repair.

This function is disabled (N) by default.

CSYNC

When enabled, this function will output a signal on the H pins suitable for use as Composite Sync. If disabled (N), then both the H & V output pins must be connected to the signal header on the monitor chassis to

drive the display. Disabling this function can be used to test a chassis with a fully separated H/V sync signal. This function setting does not take effect until exiting the menu display (Dip 5=OFF).

The OSM is always displayed with CSYNC enabled, to prevent a condition where no display results from disabling CSYNC.

This function is enabled (Y) by default.
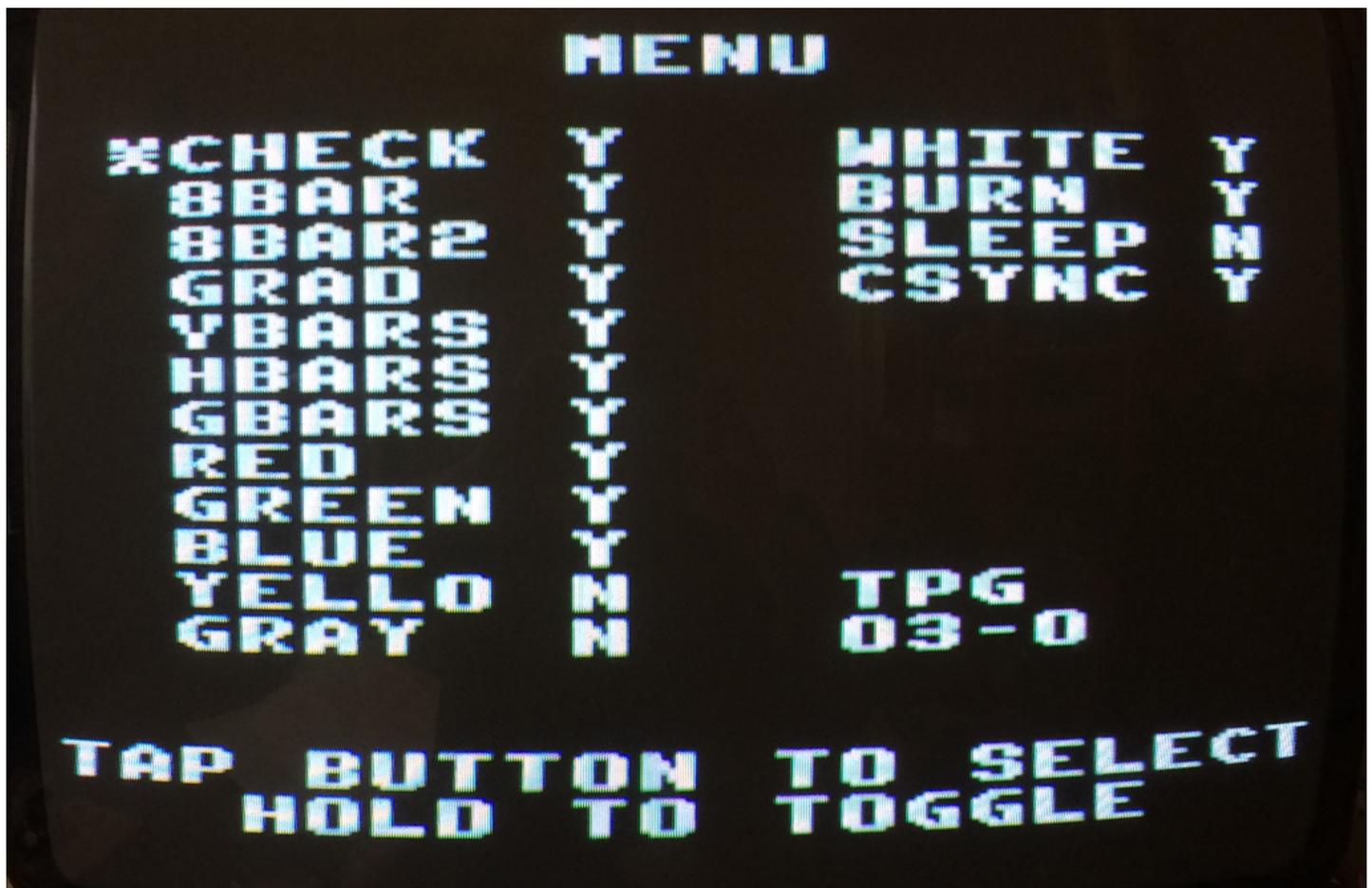
OSM screenshot with default settings. Settings are retained by internal EEPROM memory, and will persist without a battery installed. The full firmware version number is displayed in the lower right corner.

6: Firmware Programming

The TPG is equipped with a programming header for updating the firmware stored on the micro controller socketed in (G).

Pin/socket jump wires (like those used with breadboards for prototyping) can be used as an adhoc programming cable. You can find a ready supply of jumper wire on eBay, just search for "jumper wire". The pitch of the TPG programming header is .1"

To use pin/socket jump wires, connect the socket ends of the cable to the TPG programming header at (F), and insert the pin ends into the ZIF socket of a compatible EPROM programmer.

The front cover of the TPG must be removed to access the programming header. There are four screws that hold the front cover, two are visible at the top back of the unit, and two are accessed by removing the battery cover.

The programming method used to update the firmware is called "In System Programming", or ISP. The micro controller can not be flashed directly by the GQ-4X ZIF socket, since +5v and a clock signal must be present for the micro controller to receive data. By interfacing the TPG to the GQ-4X, and programming the micro controller in place, the necessary support components are present to allow the micro controller to be flashed with new data. The upshot of the ISP method is that the micro controller DIP does not have to be removed from the socket on the pcb.

PROGRAMMING GUIDE: GQ-4X

This guide will illustrate how to update the TPG firmware using a GQ-4X EPROM programmer. Other EPROM programmers will most likely require similar steps, but may differ in the terminology used.

Step 1: Launch the GQ-4X software, and select the Device type.

   The TPG micro controller will be listed as "ATMEGA88*ISP"
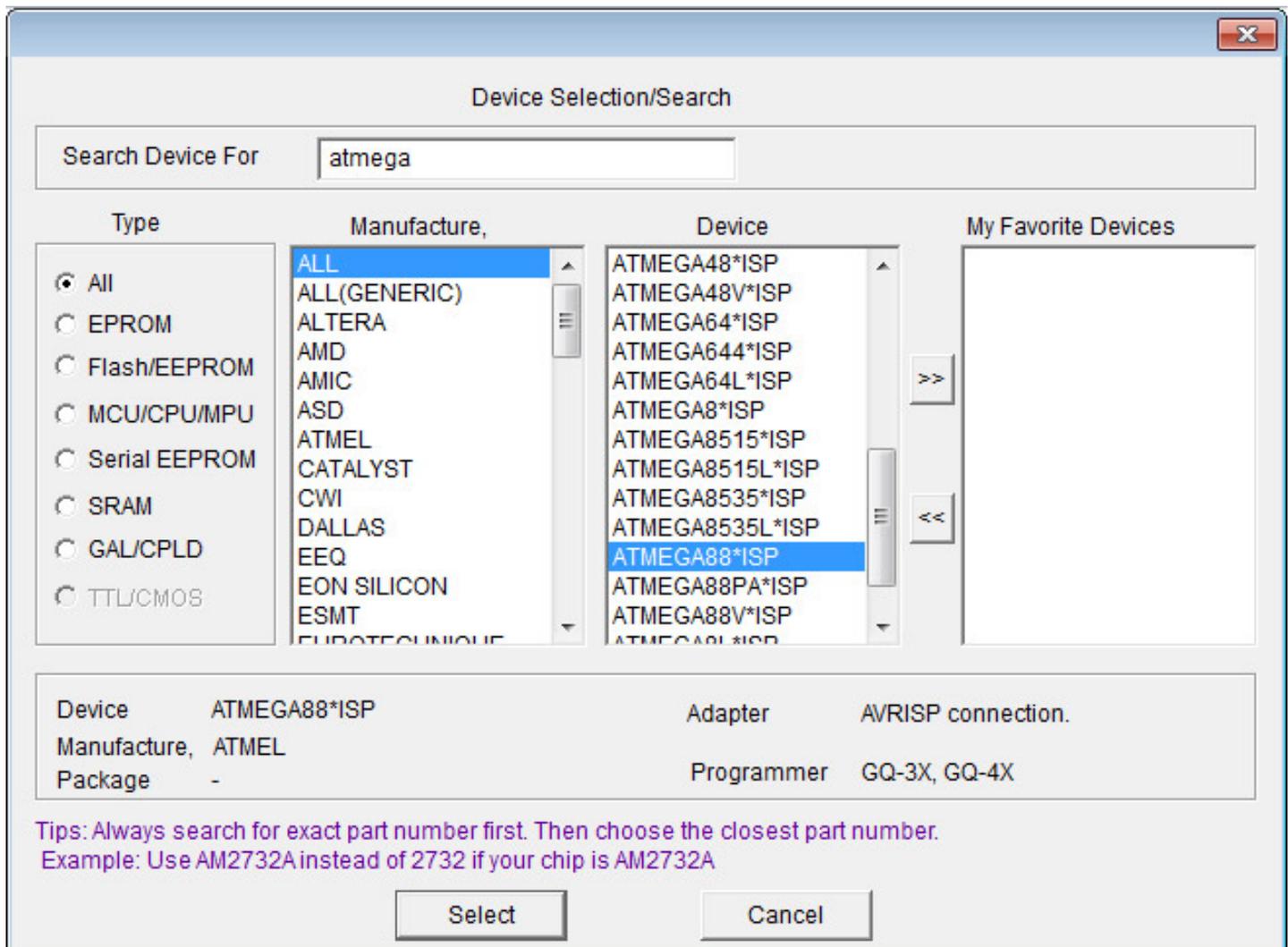
Step 2: Open the firmware .bin file.

Step 3: Connect the socket end of the programming cable to the TPG, and the pin end of the cable to the ZIF socket of the GQ-4X.

Two common color schemes for pin/socket jump wire sets are diagramed below for reference. Note the colors in the diagrams below, and match the cable colors to the pin positions in the ZIF socket & TPG programming header. See the following page for an alternate Purple/White/Black color scheme.

For additional reference, a legend is silk screened on the TPG pcb immediately to the right of the programming header.
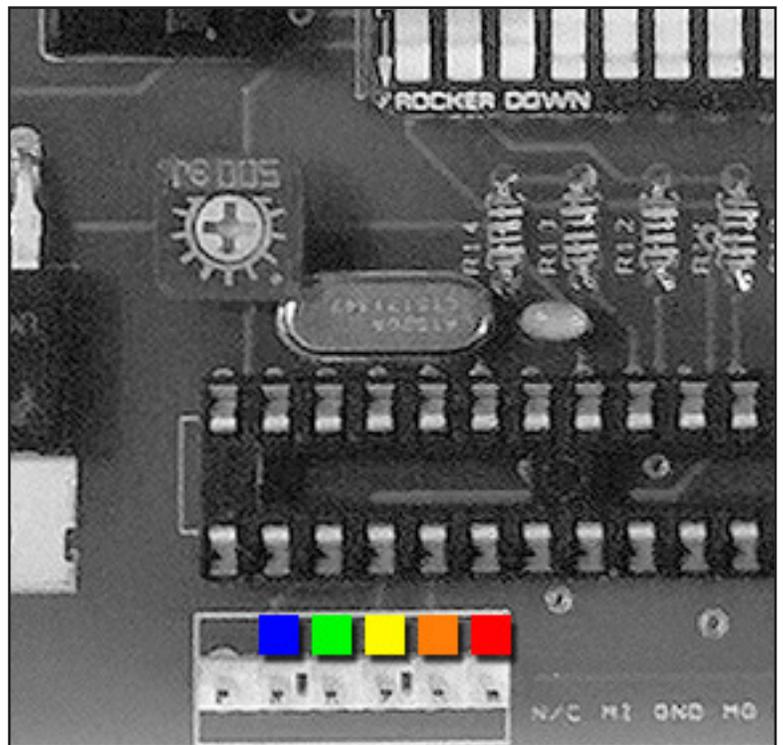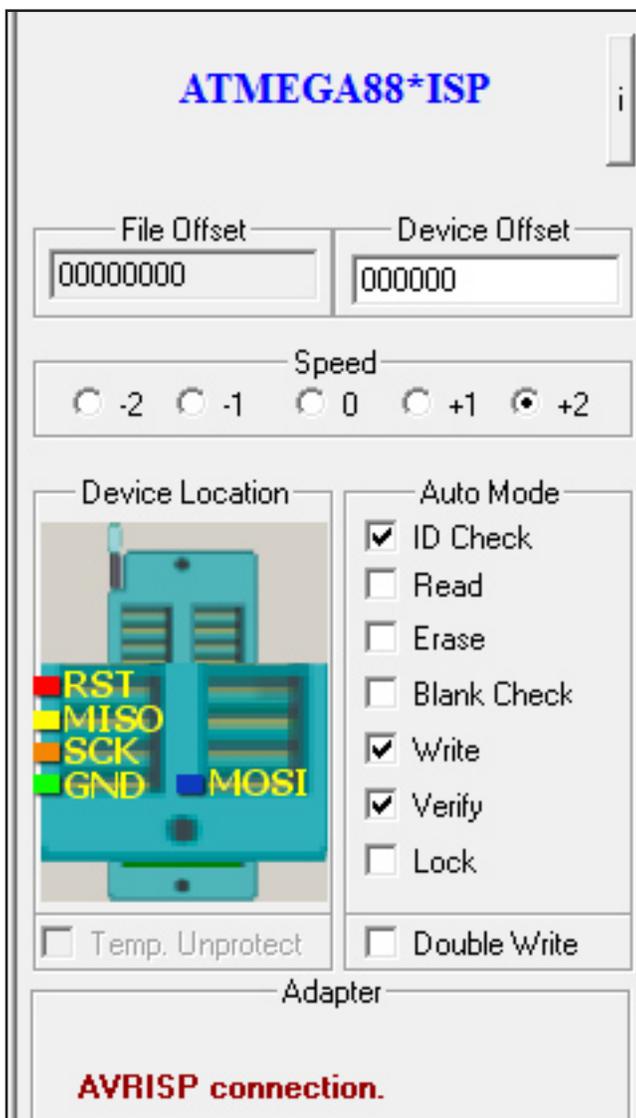
Above: TPG Programming Header

Left: ZIF diagram for ATMega 88
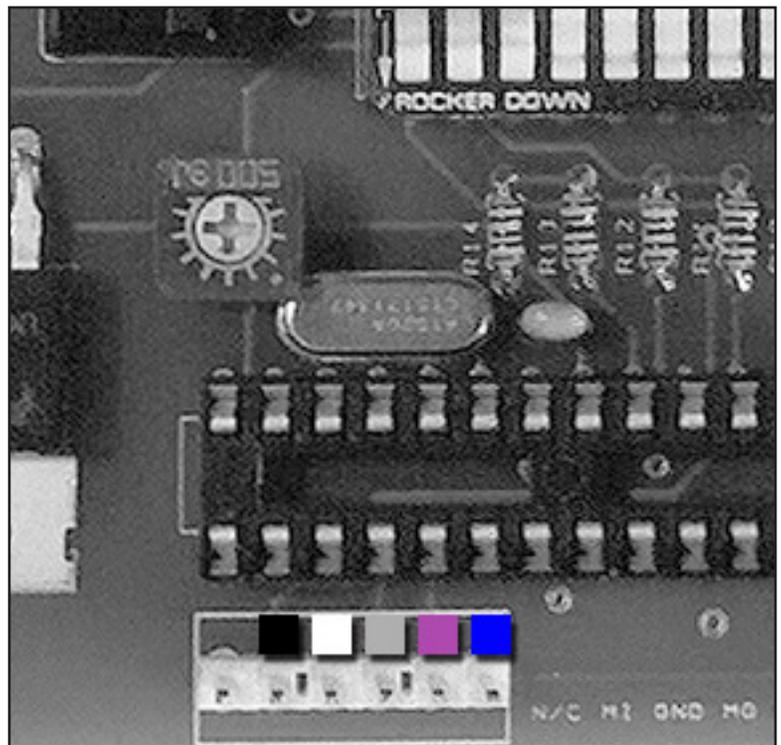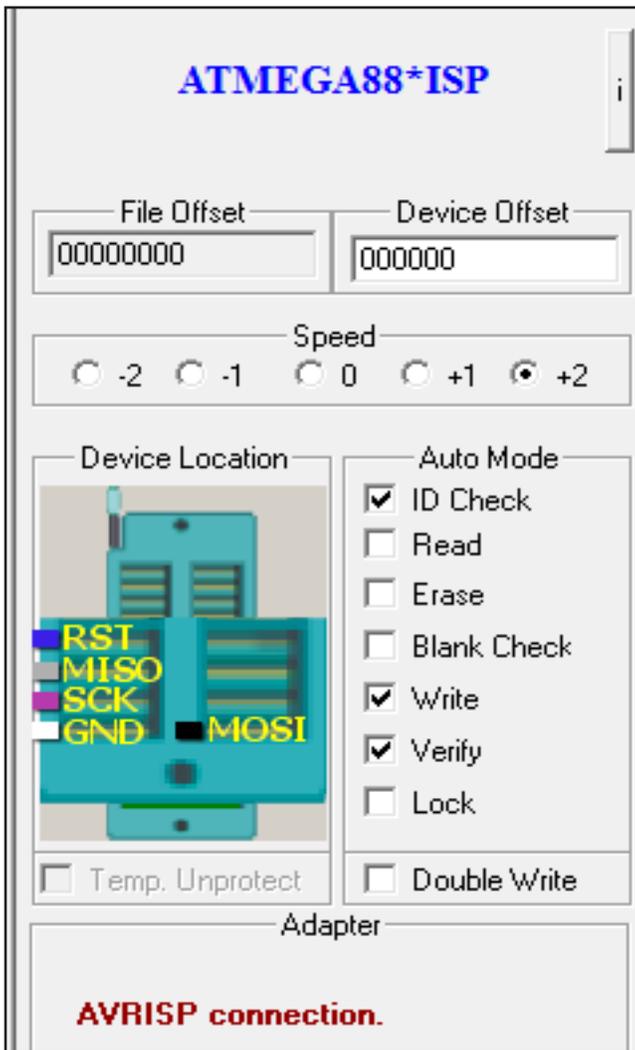
Above: TPG Programming Header

Left: ZIF diagram for ATMega 88
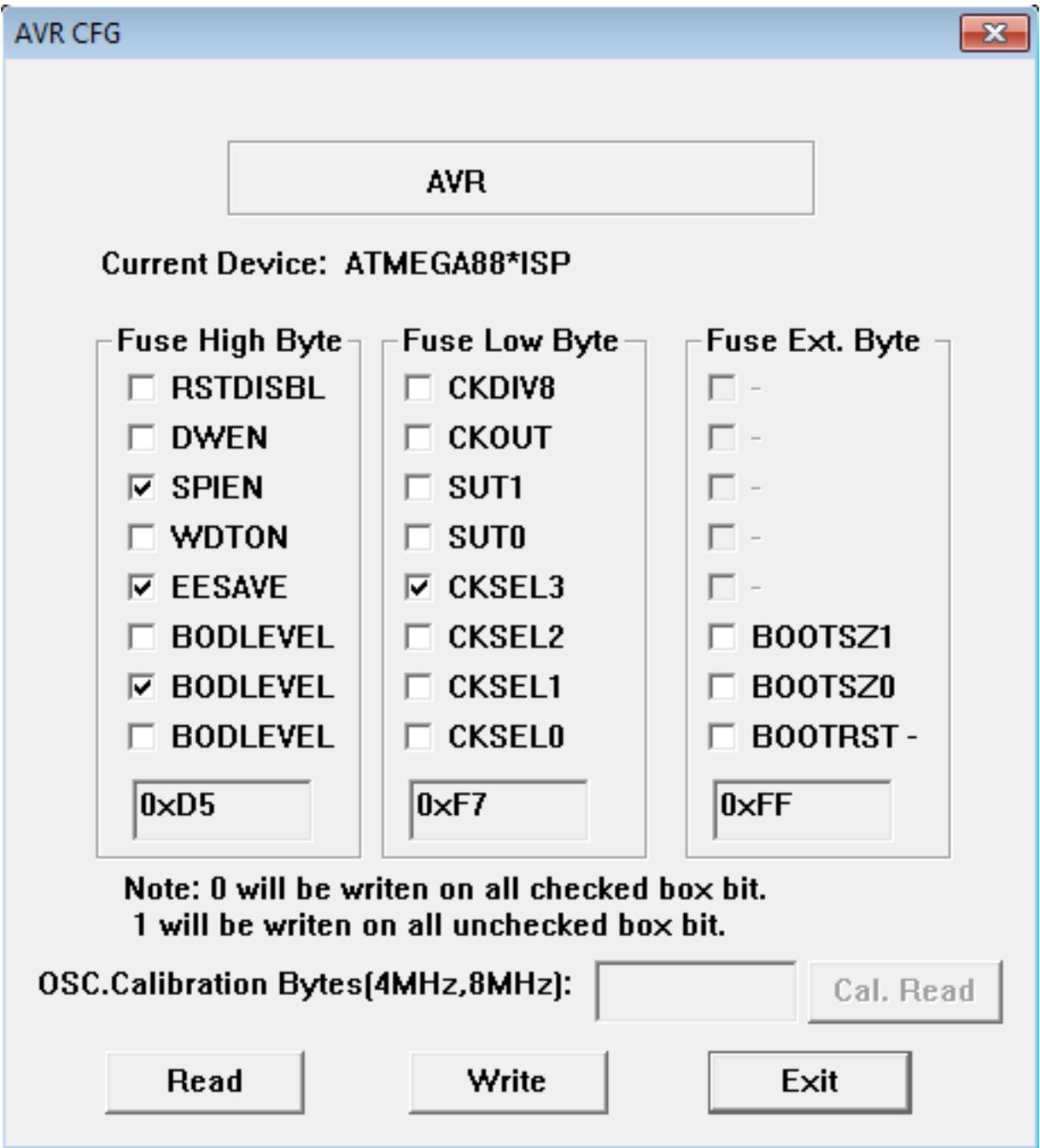
Step 4: Turn on the TPG

Step 5: Verify FUSE settings

The ATMega micro controller uses internal fuse settings for configuration. These settings may very between releases of the TPG firmware. To access the fuse settings, click the **CFG** button in the GQ-4X toolbar.

Verify that the settings depicted in the diagram on the next page match what is displayed in the *AVR CFG* dialog.

AVR CFG

AVR

Current Device: ATMEGA88*ISP

Fuse High Byte
- ☐ RSTDISBL
- ☐ DWEN
- ☑ SPIEN
- ☐ WDTON
- ☑ EESAVE
- ☐ BODLEVEL
- ☑ BODLEVEL
- ☐ BODLEVEL

0xD5

Fuse Low Byte
- ☐ CKDIV8
- ☐ CKOUT
- ☐ SUT1
- ☐ SUT0
- ☑ CKSEL3
- ☐ CKSEL2
- ☐ CKSEL1
- ☐ CKSEL0

0xF7

Fuse Ext. Byte
- ☐ -
- ☐ -
- ☐ -
- ☐ -
- ☐ -
- ☐ BOOTSZ1
- ☐ BOOTSZ0
- ☐ BOOTRST -

0xFF

Note: 0 will be writen on all checked box bit.
1 will be writen on all unchecked box bit.

OSC.Calibration Bytes(4MHz,8MHz): [   ] Cal. Read

Read   Write   Exit

If the FUSE settings need to be adjusted, click the *Write* button to update, then close the *AVR CFG* dialog.

NOTE: If all three bytes have initial values of '0xFF', the FUSE settings have not been read correctly. Verify that the TPG is powered on, and that the programming cable is properly connected to both the TPG & GQ-4X.

Step 5: Execute an Erase cycle

Step 6: Execute a Write cycle to flash the firmware file to the TPG

Step 7: Verify the Write operation.

If the Verify operation indicates a successful write then the firmware has been updated. Don't forget to turn the TPG back off!

7: Troubleshooting

Use the following guide to help solve issues you may encounter while using the TPG with an arcade monitor.

The monitor will not sync.

- Try both sync polarity combinations. It is recommended to first use -H/-V, and if the monitor will not sync, then try +H/+V.
- Check your sync connection between the TPG and chassis to ensure that the polarity matches (-sync connected to -sync input on the chassis, +sync connected to +sync input on the chassis). Most chassis follow the standard Wells Gardner input pinout (from left to right) of: R,G,B,GND,+V,+H,N/C,-V,-H
- Some chassis will not sync properly if V is connected when being fed composite sync. Turn off VSYNC (Dip 6=ON) to see if the image stablizes.
- If you are sure the sync is connected properly between the TPG & monitor chassis, then the hold/sync pot on the chassis may need to be adjusted slightly to lock in the picture. If there are two adjustment pots on the chassis, start with vertical, then horizontal hold.

No picture.

- Check that at least one of the three R,G,B Dip Switches=ON.
- Check battery voltage with a multi meter, a reading of at least +7 volts is needed to power the TPG.
- Check that the resolution switch matches the monitor type you are testing (STD or MED resolution).

The TPG frequently resets back to the Title screen.

- Battery voltage is approaching the critical point (< 7 volts), where the TPG may not work properly. Replace the battery with a fresh 9V.

The display is too dim/bright, or the contrast is too low/high.

Adjustment of the monitor chassis brightness/contrast pots may be needed, to better match the RGB signal levels of the TPG.

The TPG does not enter low power mode after 30 minutes.

- The sleep function must be enabled from the On Screen Menu. Enter the On Screen Menu by setting Dip 5=ON. Refer to Section 5 for a detailed guide to the On Screen Menu.

I don't need all the patterns, just a few.

- Individual patterns can be disabled from the On Screen Menu. Enter the On Screen Menu by setting Dip 5=ON. Refer to Section 5 for a detailed guide to the On Screen Menu.

Have a question, or issue that was not covered by the troubleshooting guide? Please send an email to support@craftymech.com, and include the firmware version of your TPG (02, 03, etc..)

8: Test Cables

The part numbers below can be used to build your own test cable for use with the TPG. The recommended length is 6', with a pair of connectors on each end (4pin + 2pin).

The connector pinout is as follows, from left to right:

4pin: R,G,B, Ground
2pin: H,V

Using a separate 2pin connector for sync allows you to easily change sync between -H/-V, and +H/+V.

Molex part numbers:

 09-50-8021 Housing, 2 pin .156" x 2

 09-50-8041 Housing, 4 pin .156" x 2

 08-50-0134 Crimp terminal .156"

Online Resellers:

 greatplainselectronics.com/products.asp?cat=86

 digikey.com

 mouser.com